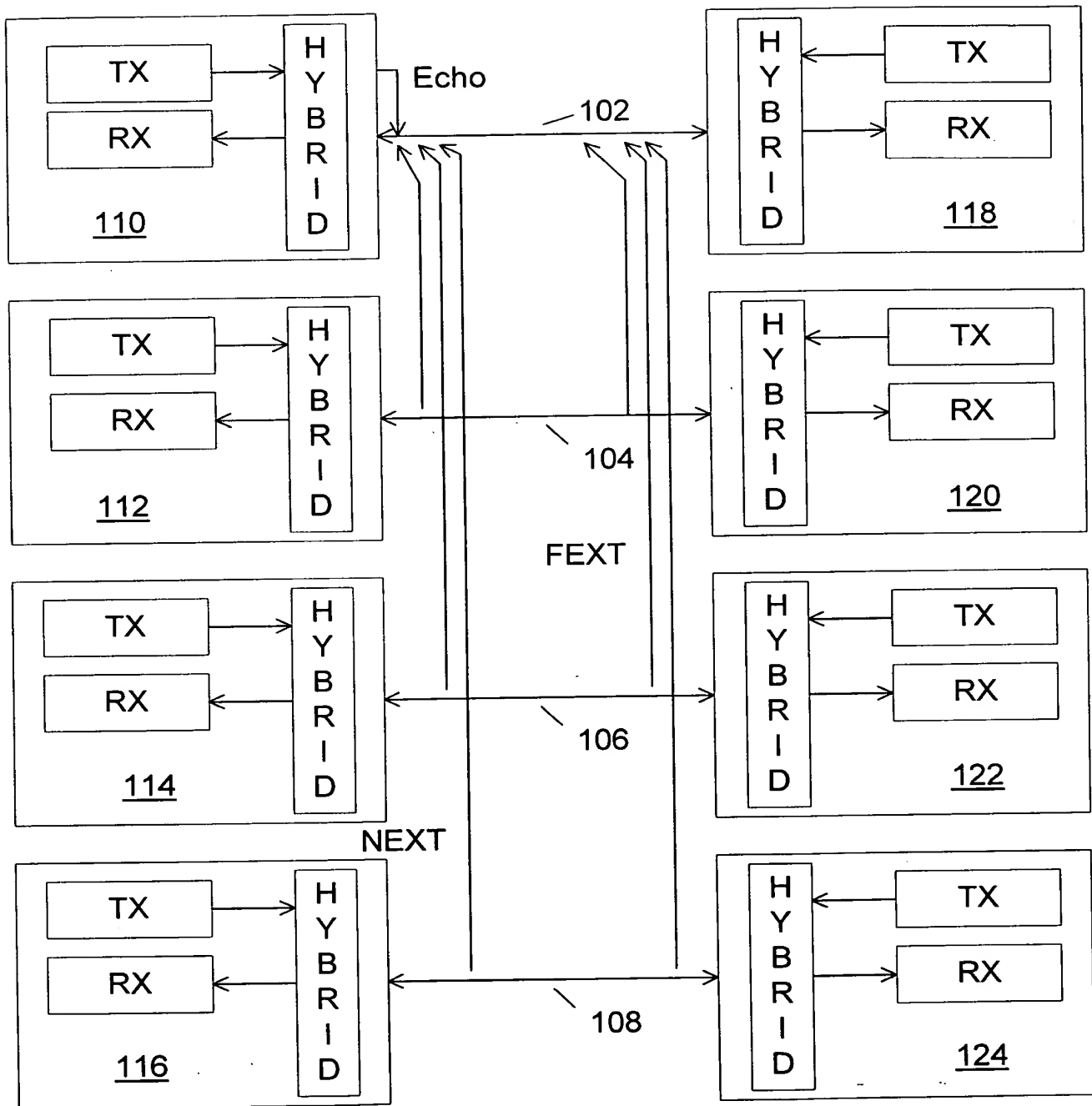


FIG. 1



The diagram illustrates a feed-forward equalizer system. An input signal X_n enters a block labeled "Channel" (202). The output of the channel is fed into a summing junction (204). This summing junction also receives input from an "Echo Canceled" block (206) and a "NEXT Canceled" block (208). The output of the summing junction is fed into a "Feed-Forward Equalizer" block (210). The output of the feed-forward equalizer is fed into another summing junction (212). This second summing junction also receives input from a "Decision-Feedback Equalizer" block (214). The output of the second summing junction is fed into a "Decision Device" (216). The output of the decision device is fed back into the "Decision-Feedback Equalizer" block (214) and also into the "Echo Canceled" block (206) and the "NEXT Canceled" block (208). The entire system is enclosed in a dashed box labeled 200.

Figure 2 – A Gigabit Ethernet Receiver

The diagram illustrates a feed-forward equalizer system. An input signal X_n enters a block labeled 'Channel' (202). The output of the channel is fed into a summing junction (204). This summing junction also receives input from an 'Echo Canceled' block (200) and a 'NEXT Canceled' block (206). The output of the summing junction is Y_n , which enters a 'Feed-Forward Equalizer' block (208). The output of the feed-forward equalizer is Z_n , which enters another summing junction. This second summing junction also receives input from a block labeled '4D-EQLFXC' (212). The output of this second summing junction enters a 'Decision Device' (22). The output of the decision device is fed back to the '4D-EQLFXC' block (212) and also branches off to the 'Echo Canceled' block (200) and the 'NEXT Canceled' block (206). A dashed box encloses the 'Echo Canceled' block (200), the 'Feed-Forward Equalizer' block (208), the '4D-EQLFXC' block (212), and the 'Decision Device' (22).

Figure 2a.

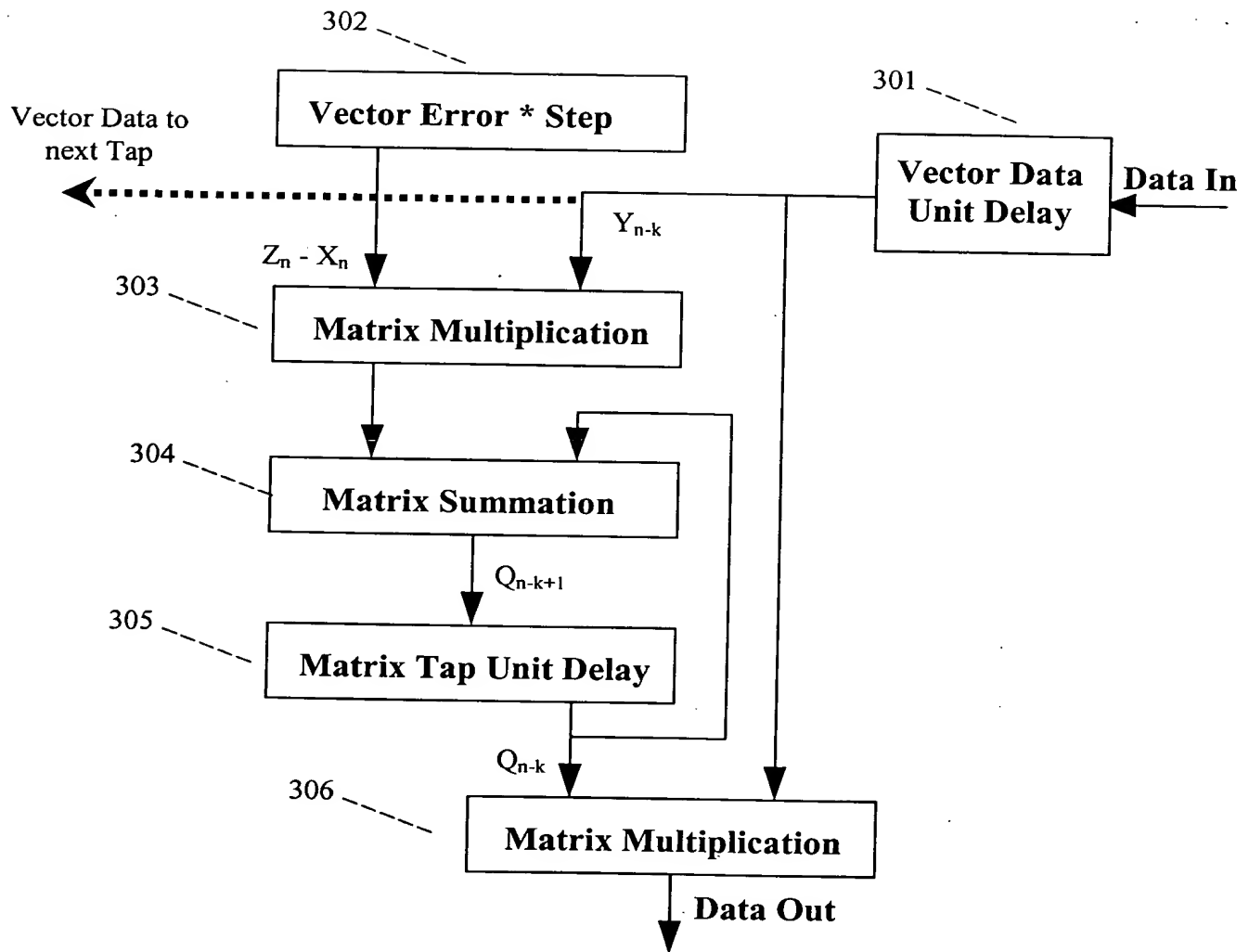


Figure 3 – A single tap of 4D-EQLFXC

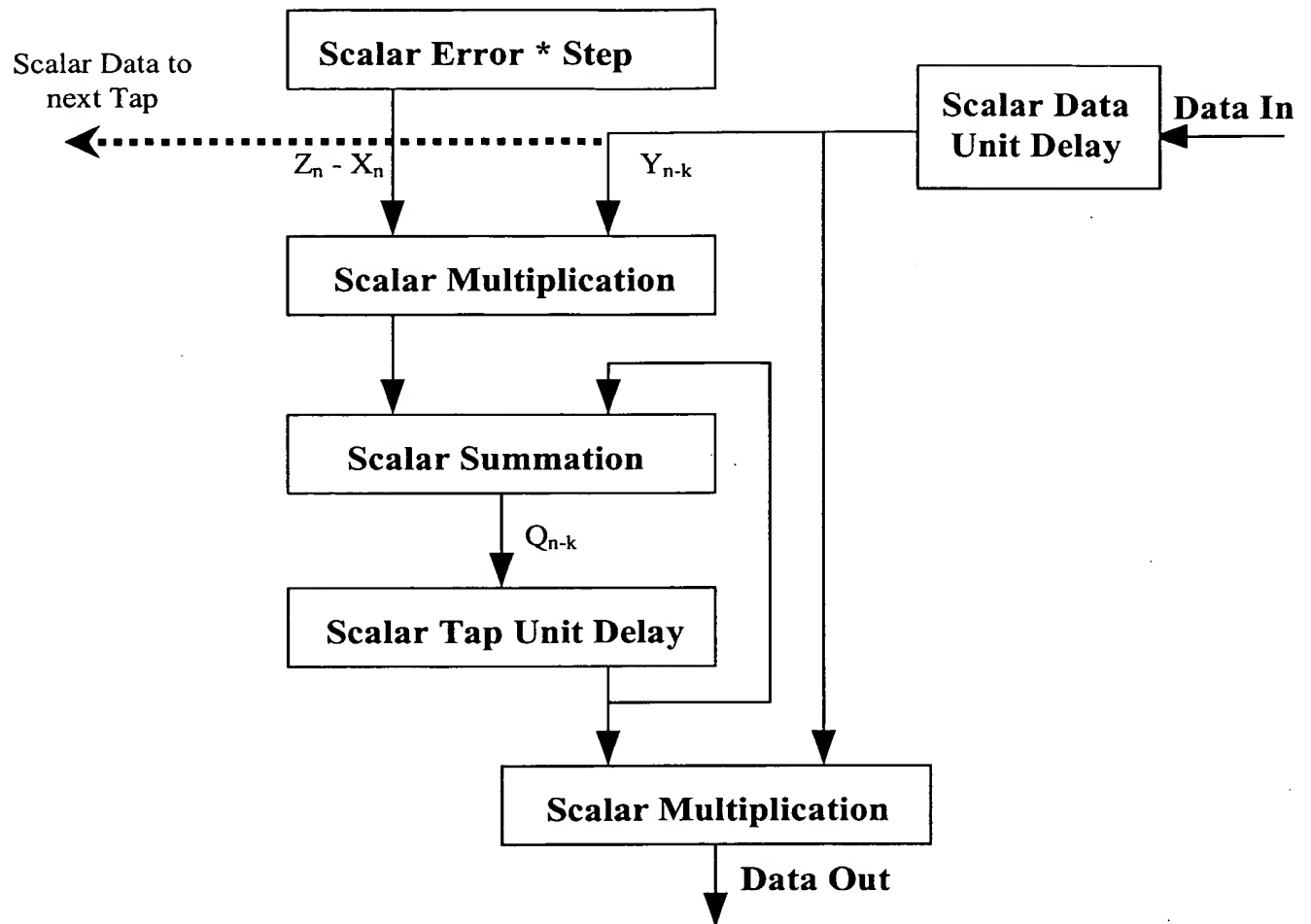


Figure 4 – A single tap of 1D-EQL

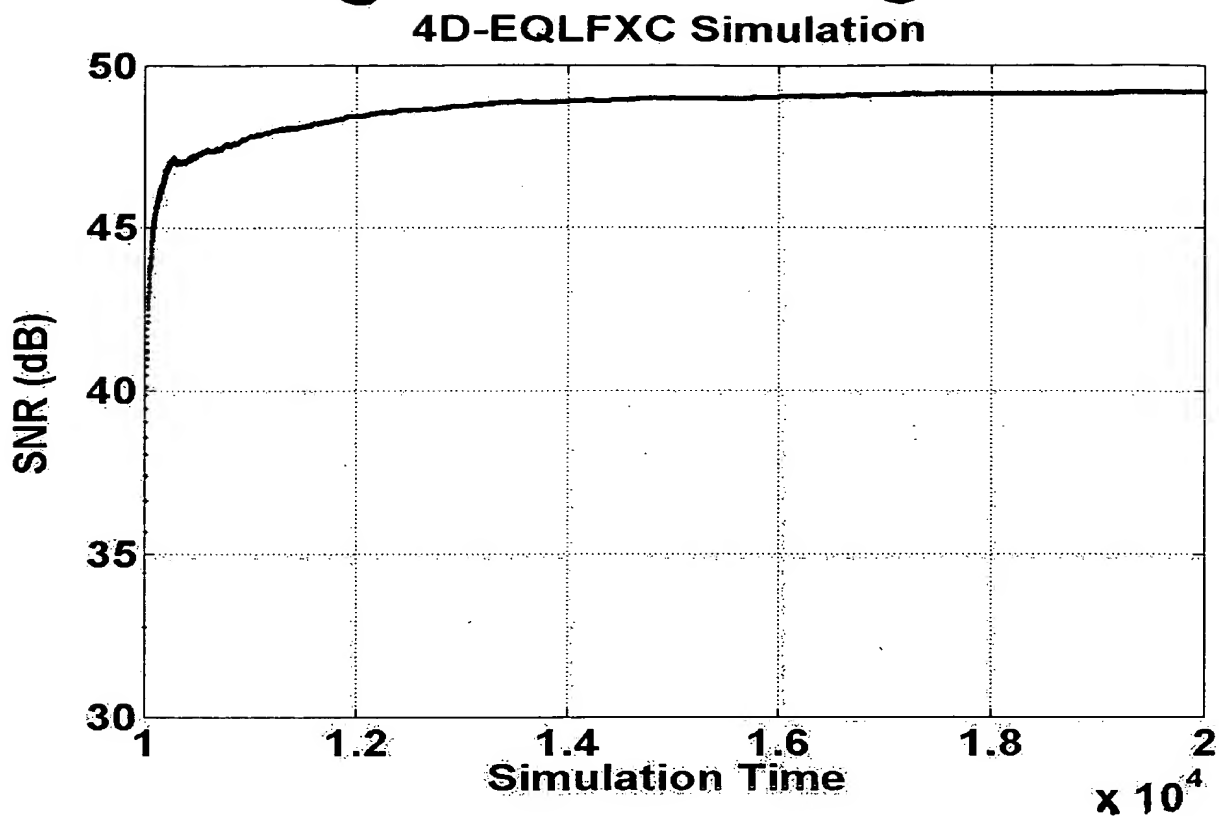


Fig. 5a

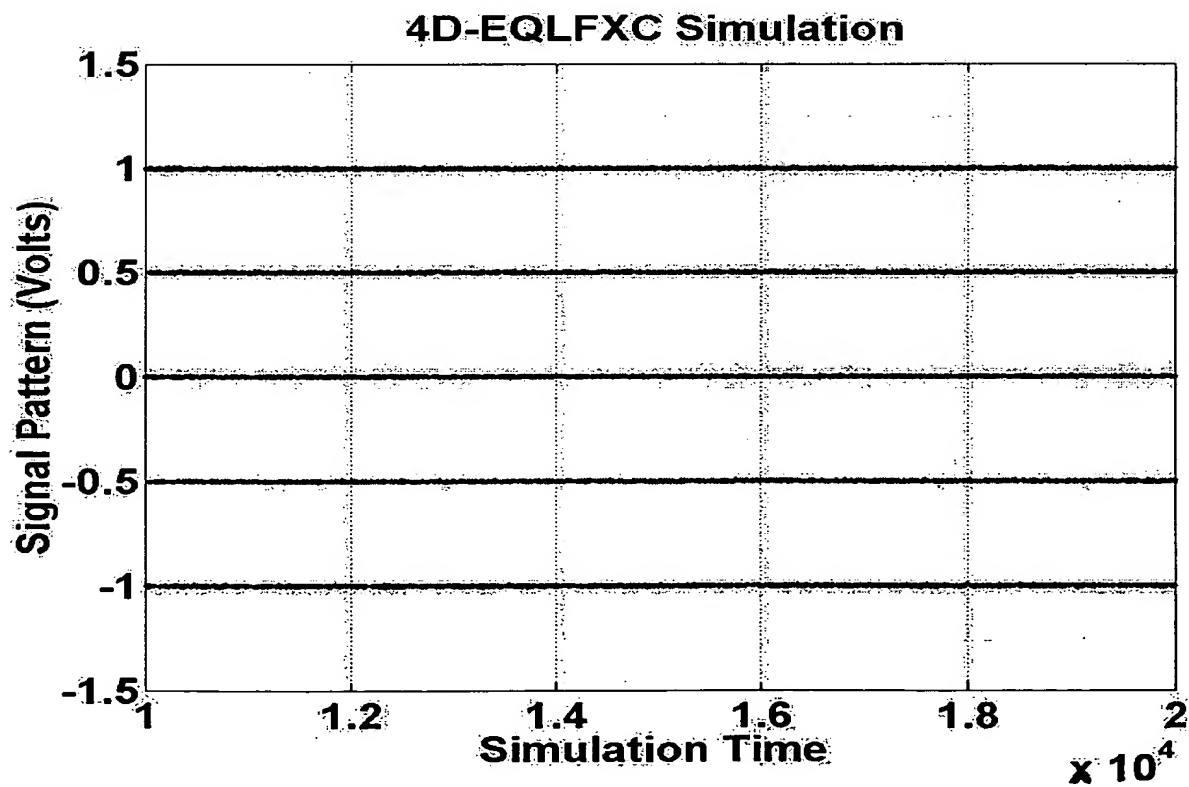


Fig. 5b

4D-EQLFXC simulation
($N=20$, $\mu=0.01$)

4 1D-EQLs Simulation

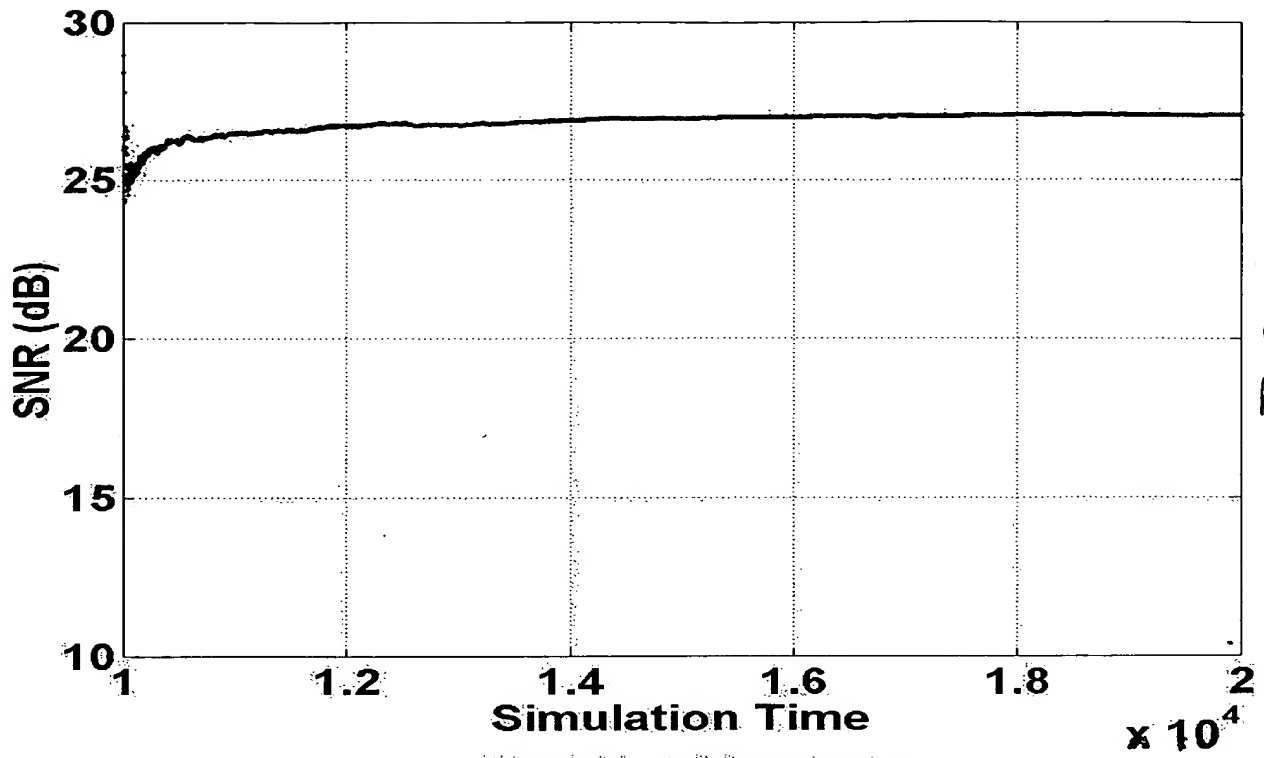


FIG. 6a
PRIOR
ART

4 1D-EQLs Simulation

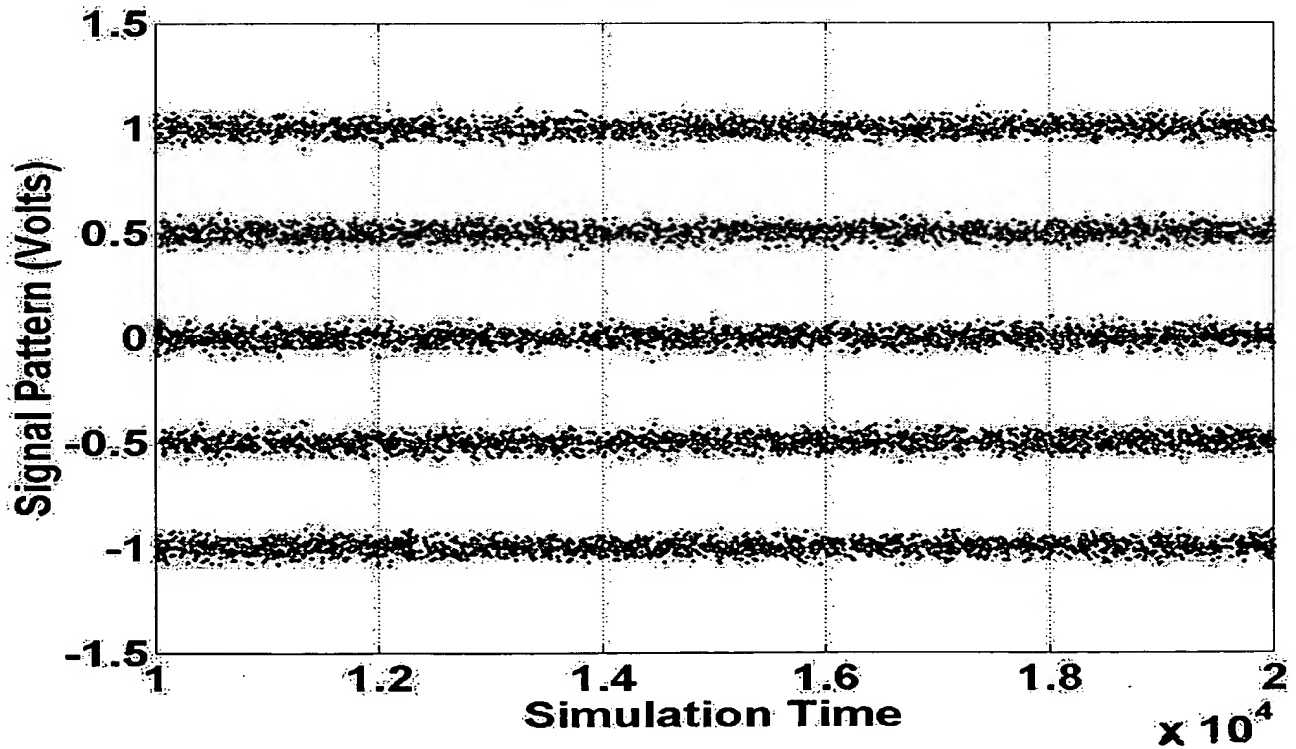


FIG. 6b
PRIOR
ART

4 1D-EQLs simulation

($N = 50$, $\mu = 0.01$)